MAXQ611 — Infrared Remote Control System-On-Chip

General Description

The MAXQ611 is a low-power, 16-bit MAXQ® microcontroller designed for low-power applications including universal remote controls, consumer electronics, and white goods. The device combines a powerful 16-bit RISC microcontroller and integrated peripherals including two universal synchronous/asynchronous receiver-transmitters (USART), SPI master/slave and I^2C communications ports, along with an IR module with carrier frequency generation and flexible port I/O capable of multiplexed keypad control.

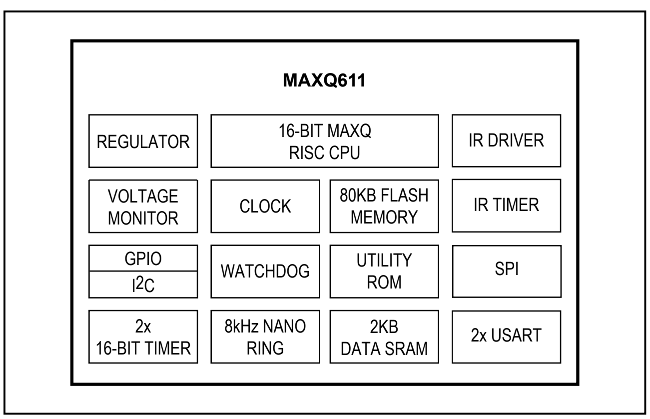
The device provides 80KB of flash memory and 2KB of data SRAM.

For the ultimate in low-power battery-operated performance, the device includes an ultra-low-power stop mode. In this mode, the minimum amount of circuitry is powered. Wake-up sources include external interrupts, the power-fail interrupt, and a timer interrupt.

Applications

- Universal Remote Controls for Tablets
- Universal Remote Controls for Smartphones

Block Diagram



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Benefits and Features

- Fast, Compact Architecture Allows Easy Integration into Applications
  - Internal 12MHz Oscillator Requires No External Components
  - Efficient, 16-Bit MAXQ20S RISC Core
  - 1.7V to 3.6V Wide Operating Range
  - 80KB Flash Program Memory
  - 2KB SRAM for Data Storage
  - Default V_{PFW} Compatible with MAXQ610
- Integrated IR Module Reduces Cost and Development Time
  - Transmit and Receive (Code Learning) Modes
  - Automatic Carrier Generation/Modulation
  - Glitch Filter Improves Noise Immunity
  - Configurable High-Current Driver
- Peripherals Support Multiple Applications
  - Up to 32 (TQFN) or 38 (Bare Die) GPIO
  - Two 16-Bit Programmable Timers/Counters Include Capture/Compare Functionality
  - SPI, I^2C, and Two USART Busses
  - Programmable Watchdog Timer Enhances System Stability
- Low Power Consumption Maximizes Battery Life
  - Power-Fail Warning Circuit Minimizes Effects of Power Fluctuation
  - Power-On and Brownout Reset Circuitry
  - 0.15μA (typ), 2.0μA (max) in Stop Mode, T_A = +25°C, Power-Fail Monitor Disabled
  - 2.0mA (typ) at 12MHz in Active Mode

***Ordering Information/Selector Guide* appears at end of data sheet.**

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, go to: www.maximintegrated.com/errata.*

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19-7309; Rev 1; 12/14

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Absolute Maximum Ratings

(All voltages with respect to GND.)
Voltage Range on V_{DD} ....-0.3V to +3.6V
Voltage Range on Any Lead Except V_{DD}....-0.3V to (V_{DD} + 0.5V)
Continuous Power Dissipation (T_A = +70°C)
TQFN (multilayer board)
(derate 37mW/°C above +70°C)................................2963mW

Operating Temperature Range.......................... -20°C to +70°C
Storage Temperature Range........................... -65°C to +150°C
Soldering Temperature (reflow).....................................+260°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA})...........27°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).................1°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(Limits are 100% tested at T_A = +25°C and T_A = +70°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER						
Supply Voltage	V_{DD}		V_{RST}		3.6	V
1.8V Internal Regulator	V_{REG18}		1.62	1.80	1.98	V
Power-Fail Warning Voltage	V_{PFW1_70}	PFWARNCN = 0000	1.65	1.70	1.75	V
	V_{PFW1_80}	PFWARNCN = 0001 (default), GBD	1.75	1.80	1.85	
	V_{PFW1_90}	PFWARNCN = 0010, GBD	1.85	1.90	1.95	
	V_{PFW2_00}	PFWARNCN = 0011, GBD	1.94	2.00	2.06	
	V_{PFW2_10}	PFWARNCN = 0100, GBD	2.04	2.10	2.16	
	V_{PFW2_20}	PFWARNCN = 0101, GBD	2.14	2.20	2.26	
	V_{PFW2_30}	PFWARNCN = 0110, GBD	2.24	2.30	2.36	
	V_{PFW2_40}	PFWARNCN = 0111, GBD	2.33	2.40	2.47	
	V_{PFW2_50}	PFWARNCN = 1000, GBD	2.43	2.50	2.57	
	V_{PFW2_60}	PFWARNCN = 1001, GBD	2.53	2.60	2.67	
	V_{PFW2_70}	PFWARNCN = 1010, GBD	2.62	2.70	2.78	
	V_{PFW2_80}	PFWARNCN = 1011, GBD	2.72	2.80	2.88	
	V_{PFW2_90}	PFWARNCN = 1100, GBD	2.82	2.90	2.98	
	V_{PFW3_00}	PFWARNCN = 1101, GBD	2.91	3.00	3.09	
	V_{PFW3_10}	PFWARNCN = 1110, GBD	3.01	3.10	3.19	
	V_{PFW3_20}	PFWARNCN = 1111, GBD	3.11	3.20	3.29	
Power-Fail Reset Voltage	V_{RST}		1.64		1.70	
Power-Fail Warning/Reset Offset	V_{PFWRST}	PFWARNCN = 0000, V_{PFW} > V_{RST}		30		mV
Power-On Reset Voltage	V_{POR}	Monitors V_{DD}		1.2		V
RAM Data Retention Voltage	V_{DRV}			1.0		V

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Active Current	I_{DD_1}	f_{SYS} = 12MHz, executing code from flash memory, all inputs connected to GND/V_{DD}, outputs do not source or sink current		2	3.7	mA
Stop Mode Current	I_{S1}	T_A = +25°C (power-fail off)		0.15	2.0	µA
		T_A = -20°C to +70°C (power-fail off)		0.15	8	
	I_{S2}	T_A = +25°C (power-fail on)		22	31	µA
		T_A = -20°C to +70°C (power-fail on)		27.6	38	
Power Consumption During Power-On Reset	I_{POR}	$V_{DD} < V_{POR}$		100		nA
Stop Mode Resume Time	t_{ON}			$3/f_{NANO} + 1024/f_{OSC}$		µs
CLOCKS						
Internal Oscillator Frequency	f_{OSC}			12		MHz
Internal Oscillator Variability	f_{OSC_VAR}	T_A = +25°C, V_{DD} = 1.8V ±5%		±0.5%		
		T_A = +25°C, V_{DD} = 1.8V			±0.5%	
		T_A = -20°C to +70°C			±1%	
System Clock Frequency	f_{SYS}	f_{OSC}/system clock divisor (1/2/4/8/256)			12	MHz
System Clock Period	t_{SYS}			$1/f_{SYS}$		
Nanopower Ring Frequency	f_{NANO}	T_A = +25°C	3.0	12.0	20.0	kHz
		T_A = +25°C, $V_{DD} = V_{POR}$	1.7	2.4		kHz
GENERAL-PURPOSE I/O AND SPECIAL FUNCTIONS						
Input Low Voltage for IRRX and All Port Pins	V_{IL}		V_{GND}		0.3 x V_{DD}	V
Input High Voltage for IRRX and All Port Pins	V_{IH}		0.7 x V_{DD}		V_{DD}	V
Input Hysteresis (Schmitt)	V_{IHYS}	V_{DD} = 3.3V, T_A = +25°C		300		mV
Output Low Voltage for All Port Pins	V_{OL}	V_{DD} = 3.6V, I_{OL} = 11mA		0.4	0.5	V
		V_{DD} = 2.35V, I_{OL} = 8mA		0.4	0.5	
		V_{DD} = 1.8V, I_{OL} = 4.5mA		0.4	0.5	
Output High Voltage All Port Pins	V_{OH}	IOH = -2mA	V_{DD} - 0.5		V_{DD}	V
Input/Output Pin Capacitance for All Port Pins	C_{IO}			15		pF
Input Leakage Current for All Pins	I_L		-100		+100	nA

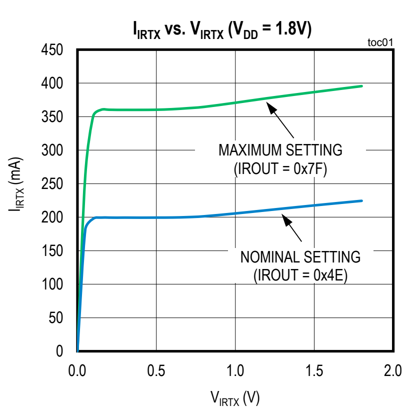
Electrical Characteristics (continued)

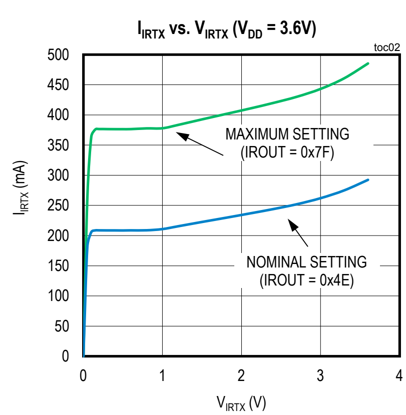
(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Pullup Resistor for $\overline{RESET}$, IRRX, and All Port Pins	R_{PU}	V_{DD} = 3.0V, V_{OL} = 0.4V	16	28	39	kΩ
		V_{DD} = 1.8V, V_{OL} = 0.4V	18	31	43	
IR MODULE WITH INTERNAL AMPLIFIER						
Input Filter Pulse-Width Reject	t_{IRRX_R}				50	ns
Input Filter Pulse-Width Accept	t_{IRRX_A}		300			ns
IRTX Sink Current	I_{IRTX}	V_{IRTX} ≥ 0.25V	200			mA
WAKE-UP TIMER						
Wake-Up Timer Interval	t_{WAKEUP}		1/ f_{NANO}		65,535/ f_{NANO}	s
FLASH MEMORY						
Flash Memory Controller Clock Frequency During Program/ Erase	f_{FP}	f_{SRC}/(FCKDIV[3:0] + 1) must equal 1MHz, verify PFI = 0 before calling utility ROM		1		MHz
Flash Mass Erase Time	t_{ME}			40		ms
Flash Page Erase Time	t_{ERASE}			40		ms
Flash Programming Time per Word	t_{PROG}	Excluding utility ROM overhead		40		µs
Write/Erase Cycles			20,000			Cycles
Data Retention		T_A = +25°C	100			Years

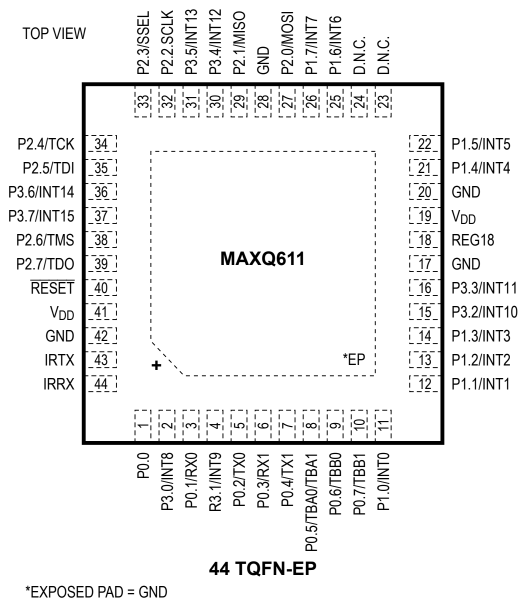
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)





Pin Configuration



Pin Description

PIN		NAME	FUNCTION
DIE	TQFN		
POWER			
24, 46	19, 41	V_{DD}	Supply Voltage. Bypass to ground with a 4.7µF capacitor.
22, 47	17, 20, 28, 42	GND	Ground. Connect directly to the ground plane.
23	18	REG18	1.8V Regulator Output. This pin must be connected to ground through a 1.0µF external capacitor. The capacitor should be placed as close to this pin as possible. No devices other than the capacitor should be connected to this pin.
—	—	EP	Exposed Pad. Connect to GND or leave electrically unconnnected.
RESET			
45	40	$\overline{\text{RESET}}$	Digital, Active-Low Reset Input/Output. The device remains in reset while this bidirectional pin is in its active state. When the pin transitions to its inactive state the device exits reset and begins execution. External circuits must be able to sink in excess of 250µA to overcome the internal pullup current source and take the pin to its active state. This pin should be left unconnected if the application does not provide a reset signal to the device. This pin is driven active as an output when an internal reset condition occurs.
IR FUNCTION			
49	44	IRRX	IR Receive Input. This pin defaults to a high-impedance input after reset.
48	43	IRTX	IR Transmit Output. This pin defaults to a high-impedance input after reset.

Pin Description (continued)

PIN		NAME	FUNCTION
DIE	TQFN		
GENERAL-PURPOSE I/O AND SPECIAL FUNCTIONS			
1	1	P0.0	P0.0: General-Purpose I/O, Port 0 Pin 0
3	3	P0.1/RX0	P0.1: General Purpose I/O, Port 0 Pin 1 RX0: USART 0 Receive
5	5	P0.2/TX0	P0.2: General-Purpose I/O, Port 0 Pin 2 TX0: USART 0 Transmit
6	6	P0.3/RX1/SCL	P0.3: General-Purpose I/O, Port 0 Pin 3 RX1: USART 1 Receive SCL: I^2C Clock
8	7	P0.4/TX1/SDA	P0.4: General-Purpose I/O, Port 0 Pin 4 TX1: USART 1 Transmit SDA: I^2C Data
9	8	P0.5/TBA0/TBA1	P0.5: General-Purpose I/O, Port 0 Pin 5 TBA0: Timer B A0 TBA1: Timer B A1
11	9	P0.6/TBB0	P0.6: General-Purpose I/O, Port 0 Pin 6 TBB0: Timer B B0
13	10	P0.7/TBB1	P0.7: General-Purpose I/O, Port 0 Pin 7 TBB1: Timer B B1
15	11	P1.0/INT0	P1.0: General-Purpose I/O, Port 1 Pin 0 INT0: External Interrupt 0
17	12	P1.1/INT1	P1.1: General-Purpose I/O, Port 1 Pin 1 INT1: External Interrupt 1
18	13	P1.2/INT2	P1.2: General-Purpose I/O, Port 1 Pin 2 INT2: External Interrupt 2
19	14	P1.3/INT3	P1.3: General-Purpose I/O, Port 1 Pin 3 INT3: External Interrupt 3
25	21	P1.4/INT4	P1.4: General-Purpose I/O, Port 1 Pin 4 INT4: External Interrupt 4
28	22	P1.5/INT5	P1.5: General-Purpose I/O, Port 1 Pin 5 INT5: External Interrupt 5
31	25	P1.6/INT6	P1.6: General-Purpose I/O, Port 1 Pin 6 INT6: External Interrupt 6
32	26	P1.7/INT7	P1.7: General-Purpose I/O, Port 1 Pin 7 INT7: External Interrupt 7
33	27	P2.0/MOSI	P2.0: General-Purpose I/O, Port 2 Pin 0 MOSI: SPI Master-Out/Slave-In
34	29	P2.1/MISO	P2.1: General-Purpose I/O, Port 2 Pin 1 MISO: SPI Master-In/Slave-Out
37	32	P2.2/SCLK	P2.2: General-Purpose I/O, Port 2 Pin 2 SCLK: SPI Clock

Pin Description (continued)

PIN		NAME	FUNCTION
DIE	TQFN		
38	33	P2.3/SSEL	P2.3: General-Purpose I/O, Port 2 Pin 3 SSEL: SPI Slave Select
39	34	P2.4/TCK	P2.4: General-Purpose I/O, Port 2 Pin 4 TCK: JTAG Clock. The POR default for the PD2.4 bit activates the weak pullup.
40	35	P2.5/TDI	P2.5: General-Purpose I/O, Port 2 Pin 5 TDI: JTAG Data In. The POR default for the PD2.5 bit activates the weak pullup.
43	38	P2.6/TMS	P2.6: General-Purpose I/O, Port 2 Pin 6 TMS: JTAG Test Mode Select. The POR default for the PD2.6 bit activates the weak pullup.
44	39	P2.7/TDO	P2.7: General-Purpose I/O, Port 2 Pin 7 TDO: JTAG Data Output. The POR default for the PD2.7 bit activates the weak pullup.
2	2	P3.0/INT8	P3.0: General-Purpose I/O, Port 3 Pin 0 INT8: External Interrupt 8
4	4	P3.1/INT9	P3.1: General-Purpose I/O, Port 3 Pin 1 INT9: External Interrupt 9
20	15	P3.2/INT10	P3.2: General-Purpose I/O, Port 3 Pin 2 INT10: External Interrupt 10
21	16	P3.3/INT11	P3.3: General-Purpose I/O, Port 3 Pin 3 INT11: External Interrupt 11
35	30	P3.4/INT12	P3.4: General-Purpose I/O, Port 3 Pin 4 INT12: External Interrupt 12
36	31	P3.5/INT13	P3.5: General-Purpose I/O, Port 3 Pin 5 INT13: External Interrupt 13
41	36	P3.6/INT14	P3.6: General-Purpose I/O, Port 3 Pin 6 INT14: External Interrupt 14
42	37	P3.7/INT15	P3.7: General-Purpose I/O, Port 3 Pin 7 INT15: External Interrupt 15
7	—	P4.0	P4.0: General-Purpose I/O, Port 4 Pin 0
10	—	P4.1	P4.1: General-Purpose I/O, Port 4 Pin 1
12	—	P4.2	P4.2: General-Purpose I/O, Port 4 Pin 2
14	—	P4.3	P4.3: General-Purpose I/O, Port 4 Pin 3
16	—	P4.4	P4.4: General-Purpose I/O, Port 4 Pin 4
26	—	P4.5	P4.5: General-Purpose I/O, Port 4 Pin 5
NO CONNECTIONS			
—	23, 24	D.N.C.	Do Not Connect. Internally connected.
27, 29, 30	—	N.C.	Do Not Connect

MAXQ611 Detailed Description

The device provides integrated, low-cost solutions that simplify the design of IR communications equipment such as universal remote controls. The internal 12MHz oscillator requires no external components. Standard features include the highly optimized, single-cycle, MAXQ, 16-bit RISC core; 80KB flash memory; 2KB data RAM; soft stack; 16 general-purpose registers; and three data pointers. The MAXQ core has the industry's best MIPS/mA rating, allowing developers to achieve the same performance as competing microcontrollers at substantially lower clock rates. Application-specific peripherals include flexible timers for generating IR carrier frequencies and modulation. A high-current IR drive pin operates with an internal receiver amplifier without external components. It also includes general-purpose I/O pins ideal for keypad matrix input, and a power-fail-detection circuit to notify the application when the supply voltage is nearing the microcontroller's minimum operating voltage.

The combination of high-performance instructions and ultra-low stop-mode current increases battery life over competing microcontrollers. An integrated POR circuit with brownout support resets the device to a known condition following a power-up cycle or brownout condition. Additionally, a power-fail warning flag is set, and a power-fail interrupt can be generated when the system voltage falls below the power-fail warning voltage, V_{PFW}. The power-fail warning feature allows the application to notify the user that the system supply is low and appropriate action should be taken.

MAXQ20S Architecture

The low-power MAXQ20S pipelined core supports the Harvard memory architecture with separate 16-bit program and data address busses. Most of the 16-bit instruction words execute in a single clock cycle with performance approaching 1MIPS per MHz.

The 16-bit data path is implemented around register modules, and each register module contributes specific functions to the core. The accumulator module consists of sixteen 16-bit registers and is tightly coupled with the arithmetic logic unit (ALU). A configurable soft stack supports program flow.

Execution of instructions is triggered by data transfer between functional register modules or between a functional register module and memory. Because data movement involves only source and destination modules, circuit switching activities are limited to active modules only. This approach localizes power dissipation and minimizes switching noise.

The MAXQ instruction set is highly orthogonal. All arithmetical and logical operations can use any register in conjunction with the accumulator. Data can be arranged in 8 or 16 bits, and movement is supported between any two registers. Memory is accessed through specific data-pointer registers with autoincrement/decrement support.

Memory

The microcontroller incorporates several memory types:

- 80KB flash memory
- 2KB SRAM data memory
- Dedicated utility ROM
- Soft stack

Memory Protection

The optional memory-protection feature segments code memory into three areas with different access privileges. This allows unique code segments to be loaded at different steps in the manufacturing process, while restricting access to higher-privilege segments that might have been loaded earlier in the process. The memory protection segments are:

- System (highest privilege)
- User-loader (medium privilege)
- User-application (lowest privilege)

Code in the system area is typically loaded by the OEM, and can be read/write protected from code executing in lower privilege segments. In a similar manner, the user-loader segment can be read/write protected from code executing in the user-application area.

Stack Memory

The MAXQ20S core provides a soft stack that can be used to store program return addresses (for subroutine calls and interrupt handling) and other general-purpose data. This soft stack is located in data memory, which means that the SRAM data memory must be shared between the soft stack and general-purpose application data storage. However, the location and size of the soft stack is determined by the user, providing maximum flexibility when allocating resources for a particular application. The stack is used automatically by the processor when the CALL, RET, and RETI instructions are executed and when an interrupt is serviced. An application can also store and retrieve values explicitly using the stack by means of the PUSH, POP, and POPI instructions.

The SP pointer indicates the current top of the stack, which initializes by default to the top of the SRAM data memory. As values are pushed onto the stack, the SP pointer decrements, which means that the stack grows downward towards the bottom (lowest address) of the data memory. Popping values off the stack causes the SP pointer value to increase.

Utility ROM

The utility ROM is located in program space beginning at address 8000h. This ROM includes the following routines:

- Production test routines (internal memory tests, memory loader, etc.), which are used for internal testing only, and are generally of no use to the end-application developer
- User-callable routines for buffer copying and fast table lookup

Following any reset, execution begins in the utility ROM at address 8000h. At this point, unless test mode has been invoked (which requires special programming through the JTAG interface), the utility ROM in the device always automatically jumps to location 0000h, which is the beginning of user application code.

Watchdog Timer

The internal watchdog timer greatly increases system reliability. The timer resets the device if software execution is disturbed. The watchdog timer is a free-running counter designed to be periodically reset by the application software. If software is operating correctly, the counter is periodically reset and never reaches its maximum count. However, if software operation is interrupted, the timer does not reset, triggering a system reset and optionally a watchdog timer interrupt. This protects the system against electrical noise or electrostatic discharge (ESD) upsets that could cause uncontrolled processor operation. The internal watchdog timer is an upgrade to older designs with external watchdog devices, reducing system cost and simultaneously increasing reliability.

The watchdog timer functions as the source of both the watchdog timer timeout and the watchdog timer reset. The timeout period is user-programmable using the WD bits as shown in Table 1. An interrupt is generated when the timeout period expires if the interrupt is enabled. All watchdog timer resets follow the programmed interrupt timeouts by 512 system clock cycles. If the watchdog timer is not restarted for another full interval in this time period, a system reset occurs when the reset timeout expires. See Table 1.

Table 1. Watchdog Timer Settings

WD (CD = 00)	PERIOD	INTERRUPT (f_{SYS} = 12MHz)	RESET (f_{SYS} = 12MHz)
00	$2^{15}/f_{SYS}$	2.7ms	2.7ms + 42.7µs
01	$2^{18}/f_{SYS}$	21.9ms	21.9ms + 42.7µs
10	$2^{21}/f_{SYS}$	174.7ms	147.7ms + 42.7µs
11	$2^{24}/f_{SYS}$	1.4s	1.4s + 42.7µs

IR Module

The IR module provides low-speed communication capability for remote control applications. Dedicated timers simplify implementation and maximize application performance. The device is used in the traditional learning circuit mode, with the receiver accepting digital input. The peripheral provides the following features:

- Transmit and receive (code learning) modes
- Automatic carrier generation/modulation
- Pulse-width glitch filter improves noise immunity
- Configurable high-current driver supports multiple LED types
- Supports receiver currents up 8µA
- Transmit frequency up to 115.2kHz

One instance of the IR peripheral is provided.

Timer/Counter Type B

Timer/counter type B is an enhanced 16-bit timer that provides input clock prescaling and pulse-width modulation (PWM) through set/reset/compare output functionality. It provides the following features:

- 16-bit timer/counter
- 16-bit up/down autoreload
- Counter function of external pulse
- 16-bit timer with capture
- 16-bit timer with compare
- Set/reset/toggle output state on comparator match
- Clock output mode
- Input/output enhancements for pulse-width modulation
- Timer input prescale option

Two instances of the peripheral are provided.

Serial Peripherals

SPI

The serial peripheral interface (SPI) is a four-wire bus providing fast, synchronous, full-duplex communications between devices. The peripheral provides the following features:

- Master or slave mode support
- Maximum SPI master transfer rate is $f_{SYS}/2$
- Maximum SPI slave transfer rate is $f_{SYS}/4$
- 8 or 16-bit data length
- Programmable clock phase and polarity
- Robust fault detection:
  - Mode fault detection
  - Write collision detection
  - Receiver overrun detection
- Programmable slave select pin polarity

One instance of the SPI peripheral is provided.

I^{2}C

The I^{2}C bus is a bidirectional, two-wire serial bus that provides a medium-speed communications network. It can operate as a one-to-one, one-to-many or many-to-many communications medium. It provides the following features:

- Master or slave mode operation
- Information transferal over a serial data circuit (SDA) and serial clock circuit (SCL)
- Supports standard (7-bit) addressing
- Support for clock stretching to allow slower slave devices to operate on higher speed busses
- Support for multiple transfer rates:
  - Standard mode: 100kbps
  - Fast mode: 400kbps
  - Fast mode plus: 1Mbps
- On-chip filter to reject spikes on the data circuit.
- Receiver FIFO depth of 2 bytes
- Transmitter FIFO depth of 2 bytes

One instance of the I^{2}C peripheral is provided.

USART

The universal synchronous/asynchronous receiver/transmitter (USART) peripheral is a two-wire, serial interface that provides fast communication between devices. It provides the following features:

- Full-duplex operation for asynchronous data transfers
- Half-duplex operation for synchronous data transfers
- Programmable interrupt when transmit or receive data operation completes
- Independent, programmable baud-rate generator
- 9th data bit can be fixed 0, 1, or used as a software parity bit
- Start and stop bits used in asynchronous modes
- Maximum frequency in synchronous mode: $f_{SRC}/4$
- Maximum frequency in asynchronous mode: $f_{SRC}/2^{21}$

Two instances of the USART peripheral are provided.

General-Purpose I/0 and External Interrupts

Port pins are provided for general-purpose I/O (GPIO) with the following features:

- CMOS output drivers
- Schmitt trigger inputs
- Optional weak pullup to V_{DD} when operating in input mode

Table 2 lists the available GPIO and external interrupts. Many GPIO pins share special functions with device peripherals and external interrupts. These special functions are listed in the *Pin Description* section, and described in the relevant user's guide section.

Table 2. MAXQ611 GPIO and External Interrupts

PACKAGE	GPIO	EXTERNAL INTERRUPTS
44 TQFN-EP	P0[7:0] P1[7:0] P2[7:0] P3[7:0]	INT[15:0]
Bare die	P0[7:0] P1[7:0] P2[7:0] P3[7:0] P4[5:0]	INT[15:0]

On-Chip Oscillator

An internal 12MHz oscillator is provided that requires no external components, thereby reducing system cost, PCB area, and radiated EMI.

Low-Power Operating Modes

The lowest power mode of operation is stop mode. In this mode, CPU state and memories are preserved, but the CPU is not actively running. Wake-up sources include external I/O interrupts, the power-fail warning interrupt, wake-up timer, or a power-fail reset. Any time the microcontroller is in a state where code does not need to be executed, the user software can put the device into stop mode. The nanopower ring oscillator is an internal ultra-low-power 8kHz ring oscillator that can drive a wake-up timer that exits stop mode. The wake-up timer is programmable by software in steps of 125μs up to approximately 8s.

The power-fail monitor is always active during normal operation.

During stop mode, the power-fail monitor can be enabled using the power-fail monitor bit (PFD). It is disabled (PFD = 1) by default after a POR. If disabled, the $V_{DD} < V_{RST}$ condition does not invoke a reset state. Regardless of the PFD bit, the $V_{DD} < V_{POR}$ condition generates a POR in stop mode.

Regardless of the state of the PFD bit, the power-fail monitor is enabled immediately prior to exiting stop mode. If a power-fail warning condition ($V_{DD} < V_{PFW}$) is then detected, the power-fail interrupt flag is set on stop mode exit. If a power-fail condition is detected ($V_{DD} < V_{RST}$), the device remains in reset and drives the RESET pin low.

Power-Fail Detection

Figure 1, Figure 2, and Figure 3 show the power-fail detection and response during normal and stop-mode operation. If a reset is caused by a power-fail, the power-fail monitor can be set to one of the following intervals:

- Always on—continuous monitoring
- 2^{11} nanopower ring oscillator clocks (~256ms)
- 2^{12} nanopower ring oscillator clocks (~512ms)
- 2^{13} nanopower ring oscillator clocks (~1.024s)

In the case where the power-fail circuitry is periodically turned on, the power-fail detection is turned on for two nanopower ring-oscillator cycles. If $V_{DD} > V_{RST}$ during detection, V_{DD} is monitored for an additional nanopower ring-oscillator period. If V_{DD} remains above V_{RST} for the third nanopower ring period, the CPU exits the reset state and resumes normal operation from utility ROM at 8000h after satisfying the crystal warmup period.

The voltage (V_{PFW}) below which a power-fail warning is generated is user configurable through the PFWARNCN bits. See the *Electrical Characteristics* table for the V_{PFW} options and corresponding PFWARNCN values.

If the RESET pin is being driven active by an external source, or a watchdog timer reset occurs, the power-fail, internal regulator, and crystal oscillator (if present) remain on during the reset event. The reset is exited in less than 20 f_{OSC} cycles after the reset source is removed.

Applications Information

The low-power, high-performance RISC architecture of this device makes it an excellent fit for many portable or battery-powered applications. It is ideally suited for applications such as universal remote controls that require the cost-effective integration of IR transmit/receive capability.

Grounds and Bypassing

Careful PCB layout significantly minimizes system-level digital noise that could interact with the microcontroller or peripheral components. The use of multilayer boards is essential to allow the use of dedicated power planes. The area under any digital components should be a continuous ground plane if possible. Keep bypass capacitor leads short for best noise rejection and place the capacitors as close as possible to the leads of the devices.

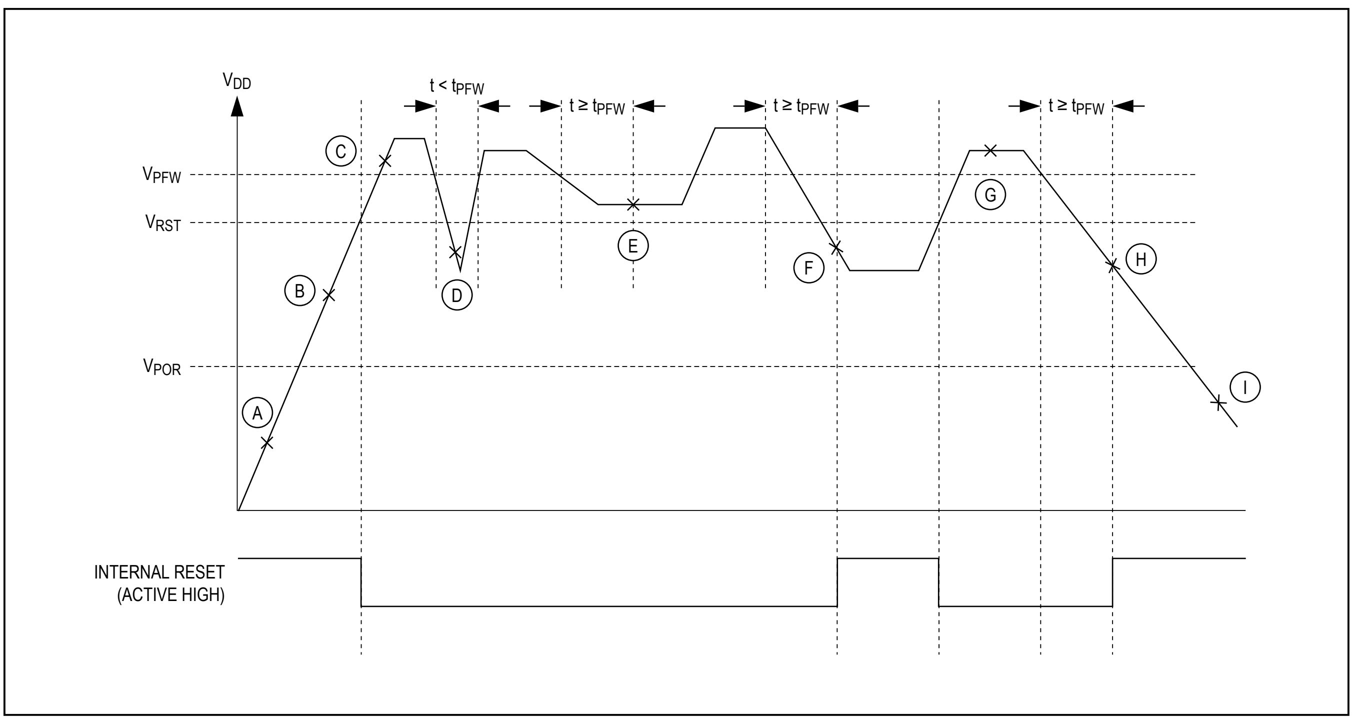


Figure 1. Power-Fail Detection During Normal Operation

Table 3. Power-Fail Detection States During Normal Operation

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
A	On	Off	Off	—	$V_{DD} < V_{POR}$.
B	On	On	On	—	$V_{POR} < V_{DD} < V_{RST}$. Crystal warmup time, t_{XTAL_RDY}. CPU held in reset.
C	On	On	On	—	$V_{DD} > V_{RST}$. CPU normal operation.
D	On	On	On	—	Power drop too short. Power-fail not detected.
E	On	On	On	—	$V_{RST} < V_{DD} < V_{PFW}$. PFI is set when $V_{RST} < V_{DD} < V_{PFW}$ and maintains this state for at least t_{PFW}, at which time a power-fail interrupt is generated (if enabled). CPU continues normal operation.
F	On (Periodically)	Off	Off	Yes	$V_{POR} < V_{DD} < V_{RST}$. Power-fail detected. CPU goes into reset. Power-fail monitor turns on periodically.
G	On	On	On	—	$V_{DD} > V_{RST}$. Crystal warmup time, t_{XTAL_RDY}. CPU resumes normal operation from 8000h.
H	On (Periodically)	Off	Off	Yes	$V_{POR} < V_{DD} < V_{RST}$. Power-fail detected. CPU goes into reset. Power-fail monitor turns on periodically.
I	Off	Off	Off	—	$V_{DD} < V_{POR}$. Device held in reset. No operation allowed.

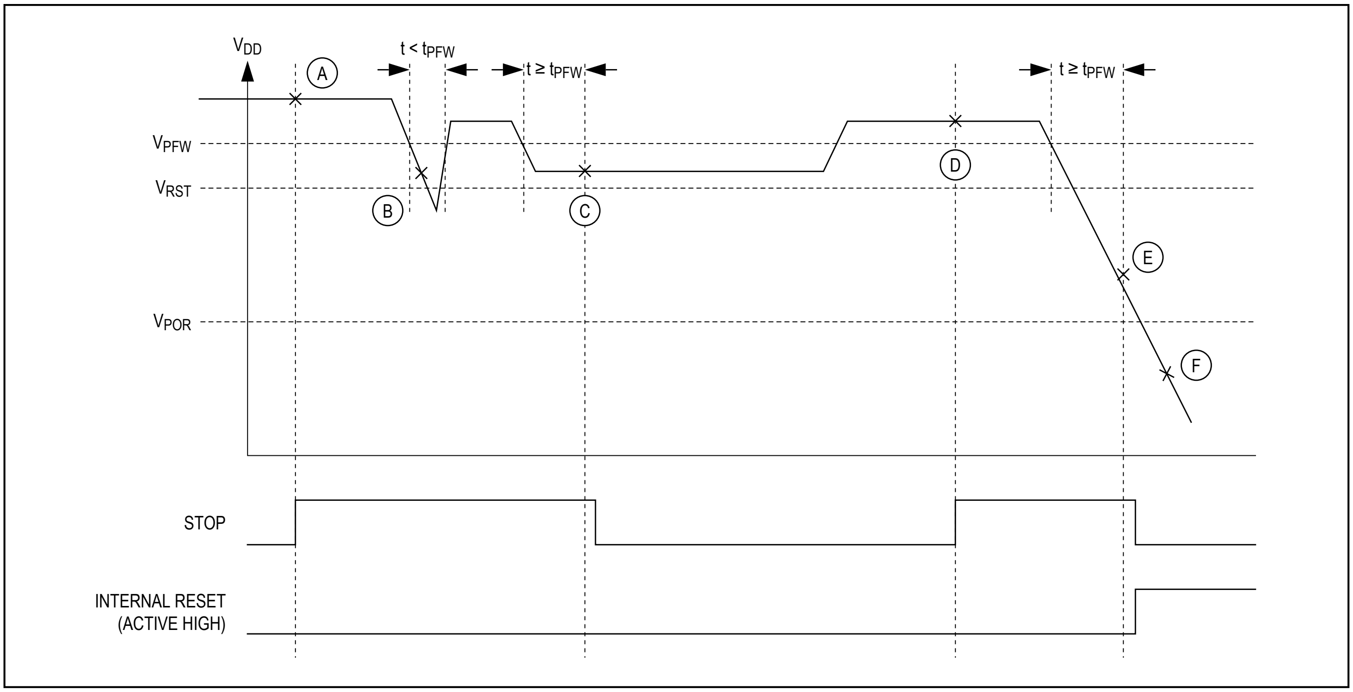


Figure 2. Stop Mode Power-Fail Detection States with Power-Fail Monitor Enabled

Table 4. Stop Mode Power-Fail Detection States with Power-Fail Monitor Enabled

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
A	On	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
B	On	Off	Off	Yes	Power drop too short. Power-fail not detected.
C	On	On	On	Yes	$V_{RST} < V_{DD} < V_{PFW}$. Power-fail warning detected. Turn on regulator and crystal. Crystal warmup time, t_{XTAL_RDY}. Exit stop mode.
D	On	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
E	On (Periodically)	Off	Off	Yes	$V_{POR} < V_{DD} < V_{RST}$. Power-fail detected. CPU goes into reset. Power-fail monitor turns on periodically.
F	Off	Off	Off	—	$V_{DD} < V_{POR}$. Device held in reset. No operation allowed.

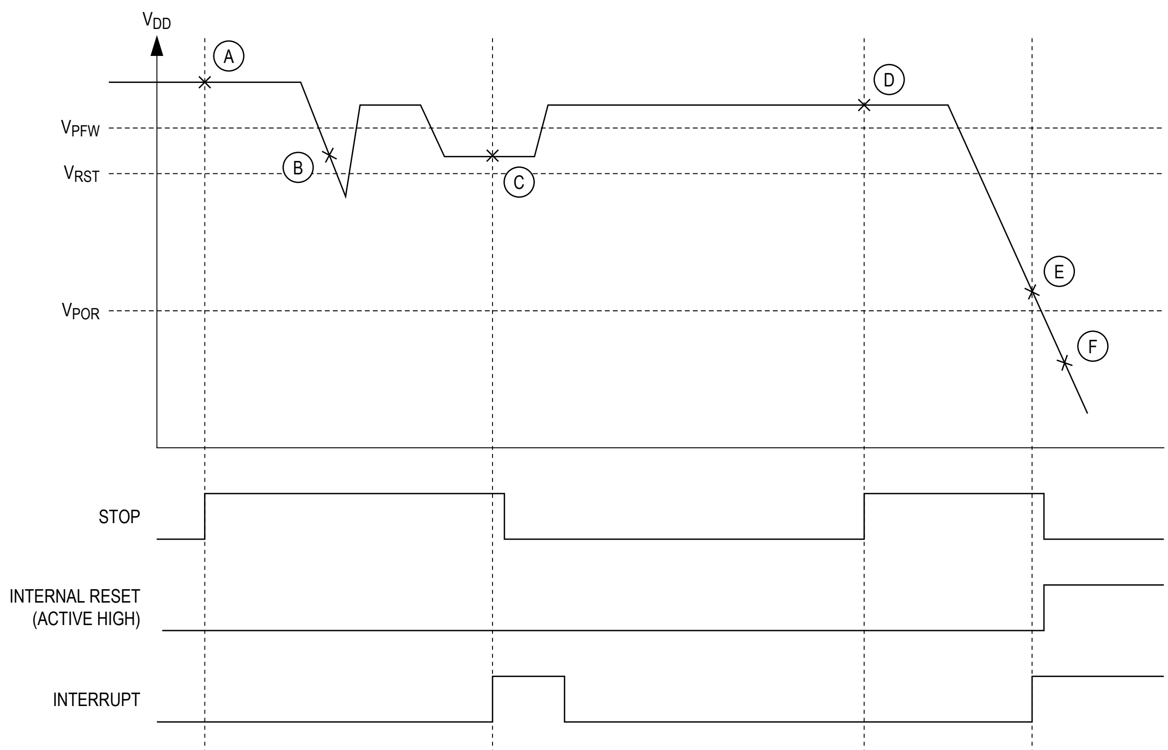


Figure 3. Stop Mode Power-Fail Detection with Power-Fail Monitor Disabled

Table 5. Stop Mode Power-Fail Detection States with Power-Fail Monitor Disabled

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
A	Off	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
B	Off	Off	Off	Yes	$V_{DD} < V_{PFW}$. Power-fail not detected because power-fail monitor is disabled.
C	On	On	On	Yes	$V_{RST} < V_{DD} < V_{PFW}$. An interrupt occurs that causes the CPU to exit stop mode. Power-fail monitor is turned on, detects a power-fail warning, and sets the power-fail interrupt flag. Turn on regulator and crystal. Crystal warmup time, t_{XTAL_RDY}. On stop mode exit, CPU vectors to the higher priority of power-fail and the interrupt that causes stop mode exit.

Table 5. Stop Mode Power-Fail Detection States with Power-Fail Monitor Disabled (continued)

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
D	Off	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
E	On (Periodically)	Off	Off	Yes	$V_{POR} < V_{DD} < V_{RST}$. An interrupt occurs that causes the CPU to exit stop mode. Power-fail monitor is turned on, detects a power-fail, and puts CPU in reset. Power-fail monitor is turned on periodically.
F	Off	Off	Off	—	$V_{DD} < V_{POR}$. Device held in reset. No operation allowed.

CMOS design guidelines for any semiconductor require that no pin be taken above V_{DD} or below GND. Violation of this guideline can result in a hard failure (damage to the silicon inside the device) or a soft failure (unintentional modification of memory contents). Voltage spikes above or below the device's absolute maximum ratings can potentially cause a devastating IC latchup.

Microcontrollers commonly experience negative voltage spikes through either their power pins or general-purpose I/O pins. Negative voltage spikes on power pins are especially problematic as they directly couple to the internal power buses. Devices such as keypads can conduct electrostatic discharges directly into the microcontroller and seriously damage the device. System designers must protect components against these transients that can corrupt system memory.

Additional Documentation

Engineers must have the following documents to fully use this device:

- This data sheet, containing pin descriptions, feature overviews, and electrical specifications.
- The device-appropriate user guide, containing detailed information and programming guidelines for core features and peripherals.
- Errata sheets for specific revisions noting deviations from published specifications.

For information regarding these documents, visit Technical Support at **support.maximintegrated.com/micro**.

Development and Technical Support

Contact technical support for information about highly versatile, affordable development tools, available from Maxim Integrated and third-party vendors.

- Evaluation kits
- Compilers
- Integrated development environments (IDEs)
- USB interface modules for programming and debugging

For technical support, go to support.maximintegrated.com/micro.

Ordering Information/Selector Guide

PART	TEMP RANGE	OPERATING VOLTAGE (V)	PROGRAM MEMORY (KB)	DATA MEMORY (KB)	GPIO	PIN-PACKAGE
MAXQ611J-XXXX+T*	-20°C to +70°C	1.70 to 3.6	80 Flash	2	32	44 TQFN-EP**
MAXQ611X-XXXX+	-20°C to +70°C	1.70 to 3.6	80 Flash	2	38	Bare die

Note: *The 4-digit suffix "-XXXX" indicates a device preprogrammed at Maxim Integrated with proprietary customer-supplied software. For more information on factory preprogramming of this device, contact Maxim Integrated at support.maximintegrated.com/micro.*

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**Future product—contact factory for availability.*

***EP = Exposed pad.*

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
44 TQFN-EP	T4477+3C	21-0144	90-0128

Appendix A

I^2C Serial Peripheral Specifications

(See Figure 4 and Figure 5.)

PARAMETER	SYMBOL	CONDITIONS	STANDARD MODE		FAST MODE		UNITS
			MIN	MAX	MIN	MAX	
Input Low Voltage	V_{IL_I2C}	Supply voltages that mismatch I^2C bus levels must relate input levels to the R_P pullup voltage	-0.5	0.3 x V_{DD}	-0.5	0.3 x V_{DD}	V
Input High Voltage	V_{IH_I2C}	Supply voltages that mismatch I^2C bus levels must relate input levels to the R_P pullup voltage	0.7 x V_{DD}		0.7 x V_{DD}	V_{DD} + 0.5V	V
Input Hysteresis (Schmitt)	V_{IHYS_I2C}	V_{DD} > 2V			0.05 x V_{DD}		V
Output Logic-Low (Open Drain or Open Collector)	V_{OL_I2C}	V_{DD} > 2V, 3mA sink current	0	0.4	0	0.4	V
Capacitive Load for Each Bus Line	C_B			400		400	pF
Output Fall Time from V_{IH_MIN} to V_{IL_MAX} with Bus Capacitance from 10pF to 400pF	t_{OF_I2C}	t_{R/F_I2C} exceeds t_{OF_I2C}, which permits RS to be connected as shown in figure		250	20 + $0.1C_B$	250	ns
Pulse Width of Spike Filtering That Must Be Suppressed by Input Filter	t_{SP_I2C}				0	50	ns
Input Current on I/O	I_{IN_I2C}	Input voltage from 0.1 x V_{DD} to 0.9 x V_{DD}	-10	+10	-10	+10	µA
I/O Capacitance	C_{IO_I2C}			10		10	pF
I^2C Bus Operating Frequency	f_{I2C}		0	100	0	400	kHz
System Frequency	f_{SYS}		0.90		3.60		MHz
I^2C Bit Rate	f_{I2C}			f_{SYS}/8		f_{SYS}/8	Hz
Hold Time After (Repeated) START	$t_{HD:STA}$		4.0		0.6		µs
Clock Low Period	t_{LOW_I2C}		4.7		1.3		µs
Clock High Period	t_{HIGH_I2C}		4.0		0.6		µs
Setup Time for Repeated START	$t_{SU:STA}$		4.7		0.6		µs

I^2C Serial Peripheral Specification (continued)

(See Figure 4 and Figure 5.)

PARAMETER	SYMBOL	CONDITIONS	STANDARD MODE		FAST MODE		UNITS
			MIN	MAX	MIN	MAX	
Hold Time for Data	$t_{HD:DAT}$	A device must internally provide a hold time of at least 300ns for $V_{IH\_I2C(MIN)}$ to bridge the undefined region of the falling edge of SCL. The maximum $t_{HD:DAT}$ needs to be met only if the device does not stretch the SCL low period	0	3.45	0	0.9	µs
Setup Time for Data	$t_{SU:DAT}$	A fast-mode I^2C bus device can be used in a standard-mode I^2C bus system; if such a device does not stretch the low period of the SCL signal, it must output the next data bit to the SDA line $t_{R\_I2C(MAX)}$ + $t_{SU:DAT}$ = 1000 + 250 = 1250ns (according to the standard-mode I^2C specification) before the SCL line is released	250		100		ns
SDA/SCL Fall Time	t_{F_I2C}			300	20 + $0.1C_B$	300	ns
SDA/SCL Rise Time	t_{R_I2C}			1000	20 + $0.1C_B$	300	ns
Setup Time for STOP	$t_{SU:STO}$		4.0		0.6		µs
Bus Free Time Between STOP and START	t_{BUF}		4.7		1.3		µs
Noise Margin at the Low Level for Each Connected Device (Including Hysteresis)	V_{nL_I2C}		0.1 x V_{DD}		0.1 x V_{DD}		V
Noise Margin at the Low Level for Each Connected Device (Including Hysteresis)	V_{nH_I2C}		0.2 x V_{DD}		0.2 x V_{DD}		V

I²C Serial Diagrams

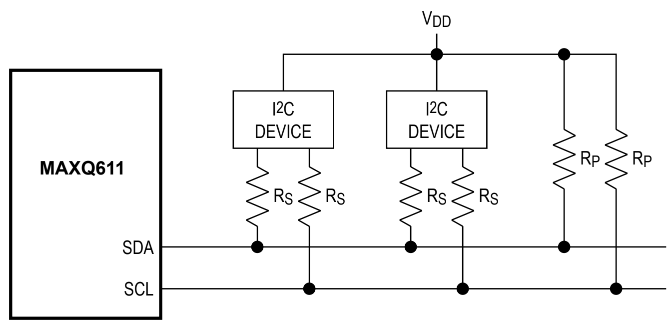
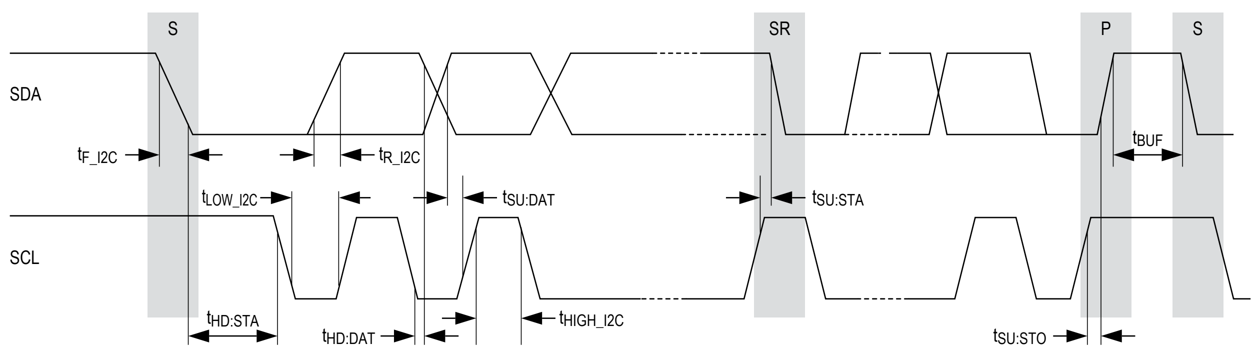


Figure 4. Series Resistors (R_S) for Protecting Against High-Voltage Spikes



NOTE: TIMING REFERENCED TO $V_{IH\_I2C(MIN)}$ AND $V_{IL\_I2C(MAX)}$.

Figure 5. I²C Bus Controller Timing Diagram

Serial Peripheral Interface (SPI) Specifications

(See Figure 6 and Figure 7.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI Master Frequency	f_{MCK}				$f_{SYS}/2$	MHz
SPI Slave Frequency	f_{SCK}				$f_{SYS}/4$	MHz
SPI Master Period	t_{MCK}			$1/f_{MCK}$		
SPI Slave Period	t_{SCK}			$1/f_{SCK}$		
SCLK Output Pulse-Width High/ Low	t_{MCH}, t_{MCL}		$t_{MCK}/2$ - 35			ns
MOSI Output Hold Time After SCLK Sample Edge	t_{MOH}		$t_{MCK}/2$ - 35			ns
MOSI Output Valid to Sample Edge	t_{MOV}		$t_{MCK}/2$ - 35			ns
MISO Input Valid to SCLK Sample Edge Rise/Fall Setup	t_{MIS}		35			ns
MISO Input to SCLK Sample Edge Rise/Fall Hold	t_{MIH}		0			ns
SCLK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}			$t_{SCK}/2$		ns
SSEL Active to First Shift Edge	t_{SSE}			50		ns
MOSI Input to SCLK Sample Edge Rise/Fall Setup	t_{SIS}		35			ns
MOSI Input from SCLK Sample Edge Transition Hold	t_{SIH}		35			ns
MISO Output Valid After SCLK Shift Edge Transition	t_{SOV}				70	ns
SCLK Inactive to SSEL Rising	t_{SD}		35			ns

SPI Timing Diagrams

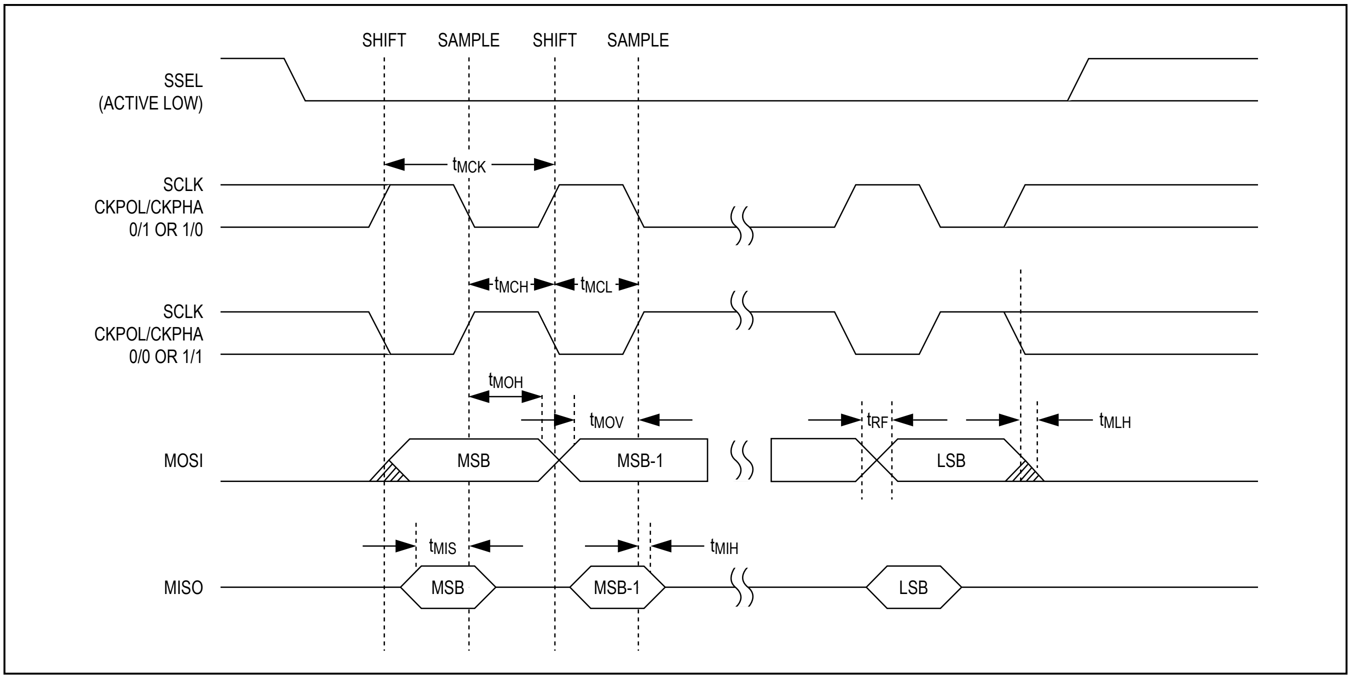


Figure 6. SPI Master Communication Timing

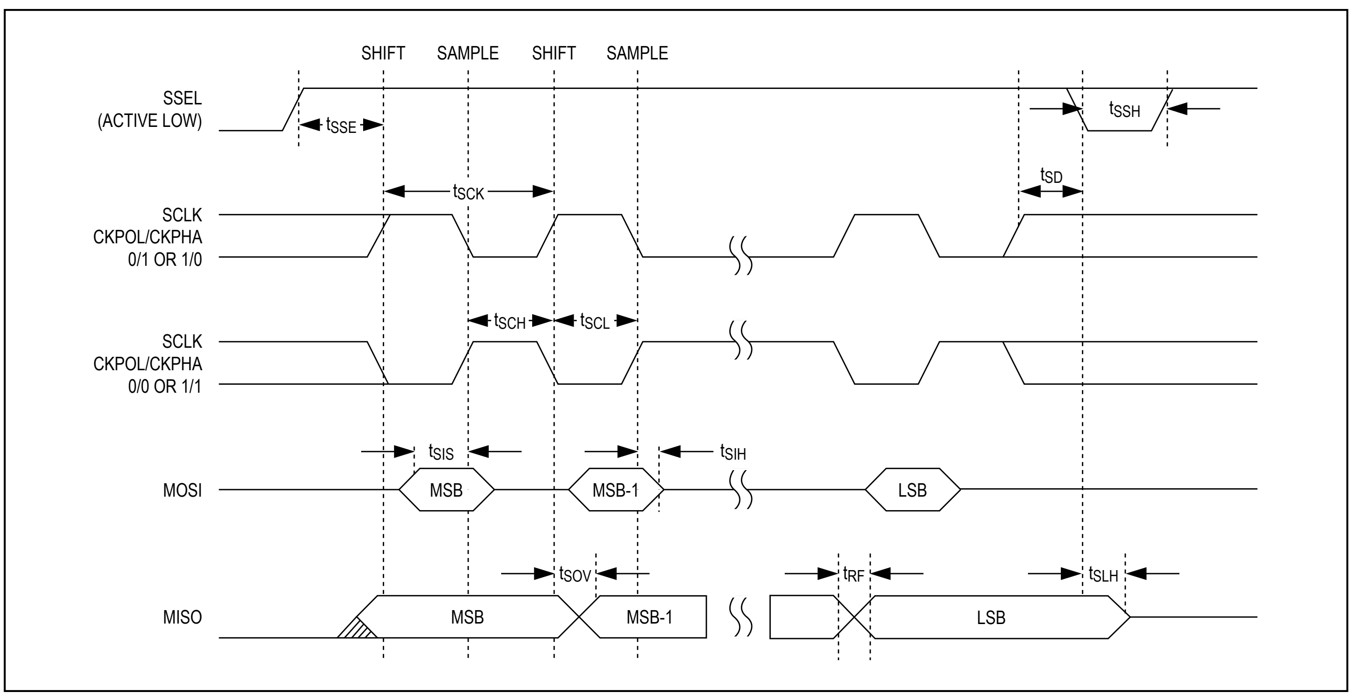


Figure 7. SPI Slave Communication Timing

USART Mode 0 Specifications

(See Figure 8.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
USART Clock Period	t_{CLCL}			$1/f_{SYS}$		
TXD Clock Period	t_{XLXL}	SM2 = 0		$12t_{CLCL}$		ns
		SM2 = 1		$4t_{CLCL}$		ns
TXD Clock High Time	t_{XHXL}	SM2 = 0		$3t_{CLCL}$		ns
		SM2 = 1		$2t_{CLCL}$		ns
RXD Output Data Valid to TXD Clock Rising Edge	t_{QVXH}	SM2 = 0		$10t_{CLCL}$		ns
		SM2 = 1		$3t_{CLCL}$		ns
RXD Output Data Hold from TXD Clock Rising Edge	t_{XHQH}	SM2 = 0		$2t_{CLCL}$		ns
		SM2 = 1		t_{CLCL}		ns
RXD Input Data Valid to TXD Clock Rising Edge	t_{DVXH}	SM2 = 0		t_{CLCL}		ns
		SM2 = 1		t_{CLCL}		ns
RXD Input Data Hold after TXD Clock Rising Edge	t_{XHDH}	SM2 = 0		t_{CLCL}		ns
		SM2 = 1		t_{CLCL}		ns

USART Timing

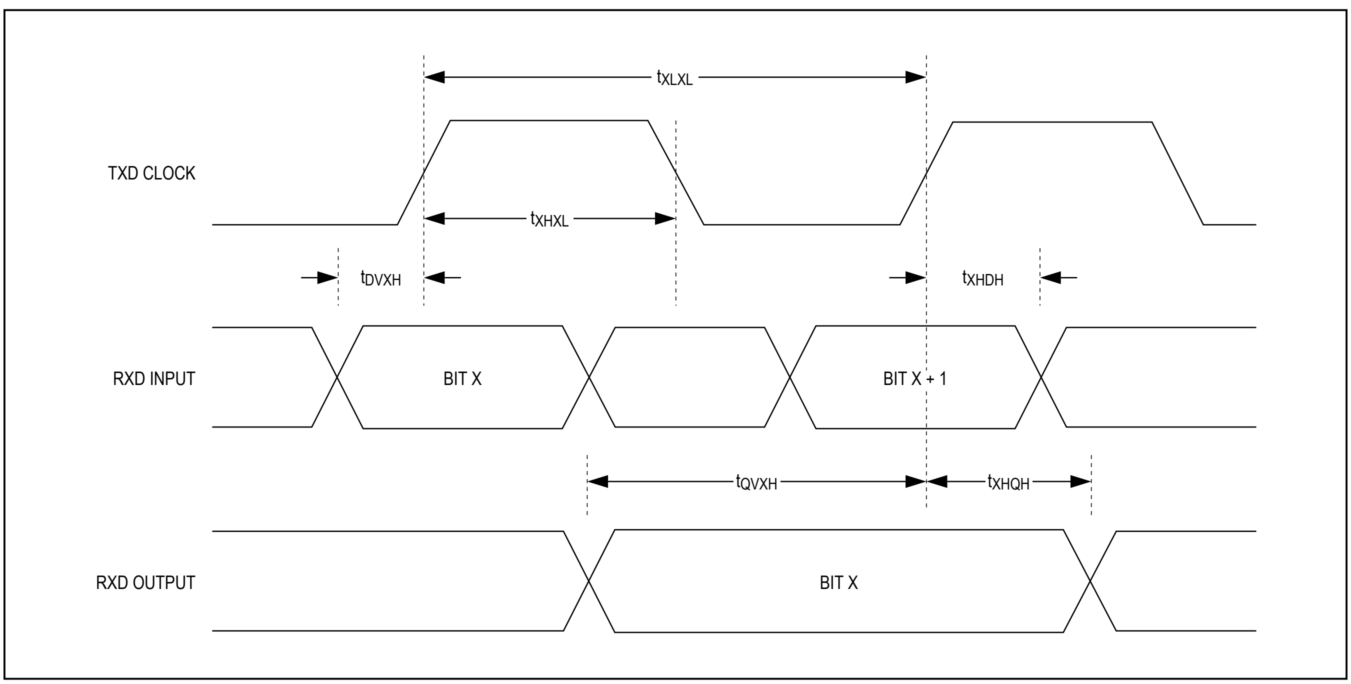


Figure 8. USART Timing Diagram

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/14	Initial release	—
1	12/14	Updated *General Description* and *Benefits and Features sections*; added *Typical Operating* Characteristics; replaced Table 2; added new Figures 1–4 and renumbered remaining figures; updated *IR Module* section; corrected part number in Figure 9	1, 4, 6–9, 13

